Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A silicon capacitor formed on an integrated circuit substrate, comprising:

a metal portion on the substrate;

a silicon nitride (SiN) portion located on the metal portion;

a silicon (Si) portion located on the silicon nitride portion; and

a second SiN portion located on the Si portion wherein the capacitor is formed using a process including depositing metal on the substrate to form the metal portion, sputtering silicon with nitrogen gas to form the SiN portion, removing nitrogen gas flow to deposit the silicon portion, and adding nitrogen gas again to form the second SiN portion.

Claim 2 (previously presented): The silicon capacitor of claim 1, wherein the silicon nitride portion is to decrease leakage.

Claim 3 (canceled)

Claim 4 (previously presented): The silicon capacitor of claim 1, further comprising a second metal portion located on the second SiN portion.

Claim 5 (canceled)

Claim 6 (previously presented): The silicon capacitor of claim 1, wherein each layer deposited is approximately forty angstroms thick.

Claims 7-14 (canceled)

Claim 15 - 18 (cancel)

Claim 19 (currently amended): An apparatus comprising:

a first metal layer located on a substrate;

a first nitride layer located directly over the first metal layer;

a silicon layer located directly over the first nitride layer;

a sandwich layer including a third nitride layer and a second silicon layer, the sandwich layer located on the silicon layer;

a second nitride layer located directly over the ~~silicon~~ sandwich layer; and

a second metal layer located directly over the second nitride layer, wherein the apparatus comprises a silicon capacitor to store charge in an integrated circuit.

Claim 20 (previously presented): The apparatus of claim 19, wherein the first nitride layer and the second nitride layer comprise silicon nitride.

Claim 21 (cancel)

Claim 22 (currently amended): ~~The~~ An apparatus ~~of claim 19, further~~ comprising:

a first metal layer located on a substrate;

a first nitride layer located directly over the first metal layer;

a silicon layer located directly over the first nitride layer;

a second nitride layer located directly over the silicon layer;

a second silicon layer located directly over the second nitride layer; ~~and~~

a third nitride layer located directly over the second silicon layer; and

a second metal layer located directly over the third nitride layer, wherein the apparatus comprises a silicon capacitor to store charge in an integrated circuit.

Claim 23 (previously presented): The apparatus of claim 19, wherein the integrated circuit comprises a mixed signal device.

Claim 24 (previously presented): The apparatus of claim 19, wherein the silicon layer comprises amorphous silicon.

Claim 25 (previously presented): The apparatus of claim 19, wherein the integrated circuit comprises a wireless multi-mode communication device.

Claim 26 (new): The apparatus of claim 22, wherein the first nitride layer and the second nitride layer comprise silicon nitride.

Claim 27 (new): The apparatus of claim 22, wherein the integrated circuit comprises a mixed signal device.

Claim 28 (new): The apparatus of claim 22, wherein the silicon layer comprises amorphous silicon.

Claim 29 (new): The apparatus of claim 22, wherein the integrated circuit comprises a wireless multi-mode communication device.